IEE PROCEEDINGS

Circuits, Devices and Systems

Vol. 146, 1999

Published by
The IEE, Savoy Place, London WC2R 0BL, United Kingdom
Publishing Department: Michael Faraday House, Six Hills Way, Stevenage, Herts. SG1 2AY, United Kingdom

IEE Proceedings

CIRCUITS, DEVICES AND SYSTEMS

The Institution of Electrical Engineers, Savoy Place, London WC2R 0BL, United Kingdom
Publishing Department: Michael Faraday House, Six Hills Way, Stevenage, Herts. SG1 2AY, United Kingdom

Volume 146 1999 UK ISSN 1350–2409

HONORARY EDITORS

Dr. P. Groeneveld (*Magma Design Automation*)
Prof. A. K. Ray (*Sheffield Hallam University*)

Pages in issues of *IEE Proc.-Circuits Devices Syst.*, 1999

Pages	Issue No.	Date
1–48	1	February
49–100	2	April
101–152	3	June
153–224	4	August
225–296	5	October
297–360	6	December

This publication is copyright under the Berne Convention and the Universal Copyright Convention. All rights reserved. Apart from any copying under the UK Copyright, Designs and Patents Act 1988, Part 1, Section 38, whereby a single copy of this article may be supplied, under certain conditions, for the purposes of research or private study, by a library of a class prescribed by The Copyright (Librarians and Archivists) (Copying of Copyright Material) Regulations 1989: SI 1989/1212, no part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means without the prior permission of the copyright owners. Permission is, however, not required to copy abstracts of individual contributions on condition that a full reference to the source is shown.

Authorisation to photocopy items for internal or personal use, or for the internal or personal use of specific clients, is granted by the Institution of Electrical Engineers for libraries and other users registered with the Copyright Clearance Center Transactional Reporting Service, provided that the base fee of $10.00 per copy is paid directly to the Copyright Clearance Center, Inc., 21 Congress Street, Salem, MA 01970, USA (1350–2409/99 $10.00). This consent does not extend to other kinds of copying, such as copying for general distribution, for advertising or promotional purposes, for creating new collective works, or for resale.

Multiple copying of the content of this publication without permission is always illegal.

The IEE is not as a body responsible for the opinions expressed by individual authors.
The IEE is a member of the Association of Learned & Professional Society Publishers.

© 1999: The Institution of Electrical Engineers

Chief Executive and Secretary of the IEE: Alf Roberts BSc PhD CEng FIEE FInstP
Managing Editor: Gill Wheeler

Printed by: Black Bear Press Limited, Cambridge, United Kingdom

Index

IEE Proceedings
Circuits, Devices and Systems

Vol. 146, 1999

Author Index

A

Abbo, A.A. p61
Al-Hashimi, B.M. p235
Almaini, A.E.A. p153
Amin, H. p225

B

Baha, B. p255
Baschirotto, A. p249
Birbas, A. p55
Board, K. p90
Bowen, T. p1
Bystrov, A. p153

C

Cappuccino, G. p16
Castello, R. p249
Cel, J. p231
Chae, S.-I. p327
Chang, C.-H. p117
Chang, M.-C. p334
Chang, T.-S. p159
Chaudhary, A. p111
Chen, C. p159
Chen, J.-M. p268
Chen, X.B. p90
Chew, K.-W. p83
Choi, I.-S. p8
Chung, Y. p139
Cocorullo, G. p16
Cook, M.J. p44
Corsonello, P. p16
Curtis, K.M. p225

D

Dabrowski, J. p77
Drew, J.D. p197
Dutta Roy, S.C. p111

F

Falkowski, B.J. p117
Friedman, E.G. p321

G

Galkowski, K. p315
Gardner, J.W. p101, p297
Garrett, D. p191
Gomez Pulido, J.A. p164
Gonzalez, J.J. p1
Gonzo, L. p184
Gottardi, M. p184
Gramacki, A. p315
Gramacki, J. p315
Grech, I. p70

H

Han, G. p105
Han, S. p105
Hassan, A.K. p44
Hatzopoulos, A.A. p350
Hayes Gill, B.R. p225
Hines, E.L. p101, p297
Ho, C.-L. p135
Ho, W.-J. p135
Hwang, S.Y. p8

J

Jagadesh Kumar, M. p291
Jayadeva p111
Jen, C.-W. p159
Jun, Y.-H. p341

K

Karmalkar, S. p211
Kim, D.-G. p327
Kinniment, D.J. p263
Kishima, A. p176
Kong, B.-S. p341
Kourtev, I.S. p321
Kurabayashi, T. p27
Kwok, H.I. p95

L

Lancaster, J.D. p235
Law, C.F. p124
Leblebici, Y. p345
Lee, H.-K. p130
Lee, T.S. p23
LeRiguer, E. p49
Liaw, J.-W. p135
Lim, J. p327
Liu, Y.X. p31, p218
Llobet, E. p101, p297

M

Maloberti, F. p184
Matsuo, T. p176
Mawby, P. p90
Mayes, D.J. p169
McCanny, J. p49
Micallef, J. p70
Milne, A. p355
Mishra, S.M. p279
Mlynek, D. p345
Moniri, M. p235
Moreno-Cadenas, J.A. p215
Murray, A.F. p169

N

Nabok, A. p44
Nishizawa, J. p27, p31, p218
Nowrouzian, B. p311

O

Okumura, K. p176
Owens, D.H. p315
Oyama, Y. p31, p218

P

Palmer, P.R. p203
Papakostas, D.K. p350
Patri, V.S. p291
Perri, S. p16
Piotka, P. p27
Plevridis, S. p55
Plotka, P. p31, p218

R

Ramakrishna, S. p211
Rao, V.M. p311
Ray, A.K. p44
Reekie, H.M. p169
Reyes-Barranca, M.A. p215
Ridge, D. p49
Rofail, S.S. p83, p124, p279
Rogers, E. p315
Rovetta, S. p108

S

Sanchez Perez, J.M. p164
Sartori, A. p184
Saunders, J. p355
Schmid, A. p345
Seng, Y.K. p279
Shoucair, F.S. p37
Simoni, A. p184
Stan, M. p191
Stark, B.H. p203
Suto, K. p31, p218

T

Talbot, A.D. p355
Tamura, K. p285
Taylor, D. p355
Tomizawa, K. p285
Torelli, G. p184
Towers, M.S. p90
Triantis, D. p55

V

Vladimirova, T. p70

W

Wang, Z.J. p95
Wei, C.-H. p268
Wilson, B. p197, p242
Wong, K.H. p148
Woods, R. p49
Wu, M.-C. p135

Y

Yakovlev, A.V. p263
Yam, Y.-O. p148
Yang, Z. p99
Yeh, C. p334
Yeo, K.-S. p83, p130
Yeo, K.S. p124

Z

Zunino, R. p108

ACOUSTICS AND ULTRASONICS

Silicon cochlea and its adaptation to spatial localisation p70

AEROSPACE SYSTEMS

VLSI data demodulator for a microwave landing system p61

AMPLIFIERS

Algorithm to calculate distortion in the common-emitter amplifier with feedback p1
Comment on "Circuit transformation method from OTA-C circuits into CFA-based RC circuits" p99
Monolithic amplifier with AGC and differential output for 622 Mbit/s optical communications p55
Transconductance feedback amplifier configuration exhibiting bandwidth-independent voltage gain p242

ANALOGUE ELECTRONICS

Analogue divider using integral compare mode and its application p105
Comment on "Circuit transformation method from OTA-C circuits into CFA-based RC circuits" p99
Compact analogue neural network: a new paradigm for neural based combinatorial optimisation p111
Estimation of statistical variables for analogue fault detectability evaluation p350
Functional-level analogue macromodelling with piecewise linear signals p77
Generation of optimised fault lists for simulation of analogue circuits and test programs p355
Minimal-connectivity circuit for analogue sorting p108
Mixed analogue-digital artificial-neural-network architecture with on-chip learning p345
Non-Gaussian kernel circuits in analogue VLSI: implications for RBF network performance p169

ARRAY SIGNAL PROCESSING

Electronic noses: a review of signal processing techniques p297

BIOMEDICAL ENGINEERING

Silicon cochlea and its adaptation to spatial localisation p70

CIRCUIT COMPONENTS

Analysis of a hysteretic circuit containing an iron-cored inductor and a semiconductor switch p176

CIRCUIT THEORY AND DESIGN

Algorithm to calculate distortion in the common-emitter amplifier with feedback p1
Analysis of a hysteretic circuit containing an iron-cored inductor and a semiconductor switch p176
Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Comment on "Circuit transformation method from OTA-C circuits into CFA-based RC circuits" p99
DC model for BiMOS structure and its adaptation to a circuit simulation environment p83
Dual nullator-norator networks p231
Estimation of statistical variables for analogue fault detectability evaluation p350
Functional-level analogue macromodelling with piecewise linear signals p77
Gate-level voltage scaling for low-power design using multiple supply voltages p334
Generation of optimised fault lists for simulation of analogue circuits and test programs p355
Modelling, decoupling and suppression of MOSFET distortion components p37
Paired Haar spectra computation through operations on disjoint cubes p117
PSPICE model for resistive gas and odour sensors p101
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Searching optimal ROBDDs using methodologies based on evolutionary algorithms p164
Semi-numerical static model for nonplanar-drift lateral DMOS transistor p139
Set of self-timed latches for high-speed VLSI p341
Synthesis of clock tree topologies to implement nonzero clock skew schedule p321
VLSI design for high-speed LZ-based data compression p268

CMOS INTEGRATED CIRCUITS

256×256-pixel CMOS digital camera for computer vision with 32 algorithmic ADCs on board p184
Altering transistor positions: impact on the performance and power dissipation of dynamic latches and flip-flops p279
Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Efficient SI wave elliptic filters based on direct and inverse Bruton transformations p235
Gate-level voltage scaling for low-power design using multiple supply voltages p334
High speed self-timed pipelined datapath for square rooting p16
Image processing chip for small object detection p49
Low-voltage fully differential switched-opamp bandpass ΣΔ modulator p249
Minimal-connectivity circuit for analogue sorting p108
New distributed arithmetic algorithm and its application to IDCT p159
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Set of self-timed latches for high-speed VLSI p341
VLSI design for high-speed LZ-based data compression p268

CODES AND DECODING

Low power parallel spread-spectrum correlator p191
VLSI design for high-speed LZ-based data compression p268

COMPUTERISED INSTRUMENTATION

Testability and test compaction for decision diagram circuits p153

CONTROL APPLICATIONS

Higher order discretisation methods for a class of 2-D continuous-discrete linear systems p315

CONTROL SYSTEM ANALYSIS

Higher order discretisation methods for a class of 2-D continuous-discrete linear systems p315

DIGITAL ARITHMETIC

5-digit overlapped-scanning technique for the modified radix-4 recoding of signed-binary numbers p311
High speed self-timed pipelined datapath for square rooting p16
New distributed arithmetic algorithm and its application to IDCT p159

DIGITAL ELECTRONICS

256×256-pixel CMOS digital camera for computer vision with 32 algorithmic ADCs on board p184
Low power, low noise micropipelined flash A-D converter p263
Low-voltage fully differential switched-opamp bandpass ΣΔ modulator p249
VLSI data demodulator for a microwave landing system p61

DIGITAL TECHNIQUES

Mixed analogue-digital artificial-neural-network architecture with on-chip learning p345

DISCRETE SYSTEMS

Higher order discretisation methods for a class of 2-D continuous-discrete linear systems p315

ENGINEERING COMPUTING

Algorithm to calculate distortion in the common-emitter amplifier with feedback p1
Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Estimation of statistical variables for analogue fault detectability evaluation p350
Functional-level analogue macromodelling with piecewise linear signals p77
Gate-level voltage scaling for low-power design using multiple supply voltages p334
Generation of optimised fault lists for simulation of analogue circuits and test programs p355
Higher order discretisation methods for a class of 2-D continuous-discrete linear systems p315
Mixed analogue-digital artificial-neural-network architecture with on-chip learning p345
Modelling, decoupling and suppression of MOSFET distortion components p37
Paired Haar spectra computation through operations on disjoint cubes p117
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Searching optimal ROBDDs using methodologies based on evolutionary algorithms p164
Semi-numerical static model for nonplanar-drift lateral DMOS transistor p139
Set of self-timed latches for high-speed VLSI p341
Synthesis of clock tree topologies to implement nonzero clock skew schedule p321
VLSI design for high-speed LZ-based data compression p268

FILTERS AND FILTERING

Comment on "Circuit transformation method from OTA-C circuits into CFA-based RC circuits" p99
Dual nullator-norator networks p231
Efficient SI wave elliptic filters based on direct and inverse Bruton transformations p235
Low-voltage BiCMOS transconductor for VHF continuous-time filters p23

IMAGE SENSORS

256×256-pixel CMOS digital camera for computer vision with 32 algorithmic ADCs on board p184

INSULATED GATE FIELD EFFECT TRANSISTORS

Modelling, decoupling and suppression of MOSFET distortion components p37
Semi-numerical static model for nonplanar-drift lateral DMOS transistor p139
Simple method for the determination of the coupling coefficient of floating-gate MOSFETs programmed with Fowler-Nordheim tunnelling p215

INTEGRATED CIRCUITS

Altering transistor positions: impact on the performance and power dissipation of dynamic latches and flip-flops p279
DC model for BiMOS structure and its adaptation to a circuit simulation environment p83
Estimation of statistical variables for analogue fault detectability evaluation p350
Functional-level analogue macromodelling with piecewise linear signals p77

Gate-level voltage scaling for low-power design using multiple supply voltages p334
Generation of optimised fault lists for simulation of analogue circuits and test programs p355
Low-power circuit implementation for partial-product addition using pass-transistor logic p124
Low-voltage BiCMOS transconductor for VHF continuous-time filters p23
Mixed analogue-digital artificial-neural-network architecture with on-chip learning p345
Monolithic amplifier with AGC and differential output for 622 Mbit/s optical communications p55
Novel 1-V full-swing high-speed BiCMOS circuit using positive feedback base-boost technique p130
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Set of self-timed latches for high-speed VLSI p341
Synthesis of clock tree topologies to implement nonzero clock skew schedule p321
Testability and test compaction for decision diagram circuits p153
VLSI design for high-speed LZ-based data compression p268

LOGIC CIRCUITS

5-digit overlapped-scanning technique for the modified radix-4 recoding of signed-binary numbers p311
Altering transistor positions: impact on the performance and power dissipation of dynamic latches and flip-flops p279
Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Gate-level voltage scaling for low-power design using multiple supply voltages p334
High speed self-timed pipelined datapath for square rooting p16
Low-power circuit implementation for partial-product addition using pass-transistor logic p124
Novel 1-V full-swing high-speed BiCMOS circuit using positive feedback base-boost technique p130
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Set of self-timed latches for high-speed VLSI p341
Testability and test compaction for decision diagram circuits p153

LOGIC DESIGN

Altering transistor positions: impact on the performance and power dissipation of dynamic latches and flip-flops p279
Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Gate-level voltage scaling for low-power design using multiple supply voltages p334
Paired Haar spectra computation through operations on disjoint cubes p117
Reduction in energy consumption by bootstrapped n MOS switches in reversible adiabatic CMOS circuits p327
Searching optimal ROBDDs using methodologies based on evolutionary algorithms p164
Set of self-timed latches for high-speed VLSI p341
Synthesis of clock tree topologies to implement nonzero clock skew schedule p321
Testability and test compaction for decision diagram circuits p153
VLSI design for high-speed LZ-based data compression p268

MATHEMATICAL TECHNIQUES

Compact analogue neural network: a new paradigm for neural based combinatorial optimisation p111

MEASUREMENT OF SPECIFIC VARIABLES

PSPICE model for resistive gas and odour sensors p101

MICROPROCESSORS

Image processing chip for small object detection p49
New distributed arithmetic algorithm and its application to IDCT p159
VLSI design for high-speed LZ-based data compression p268

MODULATION

Innovative demodulation method for SSB technique p148
Transmission of wideband DC-coupled analogue signals over fibre p197

MODULATORS AND DEMODULATORS

VLSI data demodulator for a microwave landing system p61

NEURAL NETWORKS

Compact analogue neural network: a new paradigm for neural based combinatorial optimisation p111
Electronic noses: a review of signal processing techniques p297
Image processing chip for small object detection p49
Minimal-connectivity circuit for analogue sorting p108
Mixed analogue-digital artificial-neural-network architecture with on-chip learning p345
Non-Gaussian kernel circuits in analogue VLSI: implications for RBF network performance p169
Two-ring systolic array network for artificial neural networks p225

NUMERICAL ANALYSIS

Analysis of a hysteretic circuit containing an iron-cored inductor and a semiconductor switch p176
Comparative study of balance equation models p285
New distributed arithmetic algorithm and its application to IDCT p159
Paired Haar spectra computation through operations on disjoint cubes p117
Simple method for the determination of the coupling coefficient of floating-gate MOSFETs programmed with Fowler-Nordheim tunnelling p215

OPTICAL COMMUNICATION

Transmission of wideband DC-coupled analogue signals over fibre p197

OPTICAL COMMUNICATION EQUIPMENT

Monolithic amplifier with AGC and differential output for 622 Mbit/s optical communications p55

OPTICAL IMAGE PROCESSING

Image processing chip for small object detection p49

OPTICAL MATERIALS

Photoconduction in Langmuir-Blodgett films of octasubstituted metal-free phthalocyanine molecules p44

OPTIMISATION

Circuit partitioning algorithm for low-power design under area constraints using simulated annealing p8
Searching optimal ROBDDs using methodologies based on evolutionary algorithms p164
Synthesis of clock tree topologies to implement nonzero clock skew schedule p321
Testability and test compaction for decision diagram circuits p153

PARALLEL PROCESSING

Low power, low noise micropipelined flash A-D converter p263
Two-ring systolic array network for artificial neural networks p225
VLSI design for high-speed LZ-based data compression p268

POWER ELECTRONICS

Analysis and control of a cross-regulated multi-output forward quasi-resonant converter p255
Analysis of a hysteretic circuit containing an iron-cored inductor and a semiconductor switch p176
Formalised method for effecting multiple modes in single MOS gated power devices p203
High-voltage sustaining structure with embedded oppositely doped regions p90

RADIO SYSTEMS

Low power parallel spread-spectrum correlator p191

SEMICONDUCTOR DEVICE MODELLING

Comparative study of balance equation models p285
HEMT modelling using semi-physical expressions for the equilibrium space-charge parameters of the modulation-doped heterojunction p211
Modelling, decoupling and suppression of MOSFET distortion components p37
Novel Ge-profile design for high-speed SiGe HBTs: modelling and analysis p291
Semi-numerical static model for nonplanar-drift lateral DMOS transistor p139
Simple method for the determination of the coupling coefficient of floating-gate MOSFETs programmed with Fowler-Nordheim tunnelling p215
Systematic approach to modelling and parameter extraction of an ion-implanted GaAs MESFET p95
Tunnelling current analysis of GaAs n^{++}-p^{++}-n^{++} ultrathin barrier structures grown by molecular layer epitaxy p218

SEMICONDUCTOR DEVICES

Comparative study of balance equation models p285
Formalised method for effecting multiple modes in single MOS gated power devices p203
GaAs MESFET with low current capability grafted onto quartz substrate p135
HEMT modelling using semi-physical expressions for the equilibrium space-charge parameters of the modulation-doped heterojunction p211
Light emission from tunnelling mode GaAs static induction transistor p27
Novel Ge-profile design for high-speed SiGe HBTs: modelling and analysis p291
Systematic approach to modelling and parameter extraction of an ion-implanted GaAs MESFET p95
Tunnelling current analysis of GaAs n^{++}-p^{++}-n^{++} ultrathin barrier structures grown by molecular layer epitaxy p218
Tunnelling currents in very thin planar-doped barrier n^+-i-p^+-i-n^+ structures p31

SEMICONDUCTOR INTERFACES

Modelling, decoupling and suppression of MOSFET distortion components p37

SEMICONDUCTOR MATERIALS

Photoconduction in Langmuir-Blodgett films of octasubstituted metal-free phthalocyanine molecules p44
Tunnelling current analysis of GaAs n^{++}-p^{++}-n^{++} ultrathin barrier structures grown by molecular layer epitaxy p218
Tunnelling currents in very thin planar-doped barrier n^+-i-p^+-i-n^+ structures p31

SENSORS AND ACTUATORS

Electronic noses: a review of signal processing techniques p297
PSPICE model for resistive gas and odour sensors p101

SIGNAL PROCESSING

Electronic noses: a review of signal processing techniques p297
Low power parallel spread-spectrum correlator p191
VLSI design for high-speed LZ-based data compression p268

STATISTICAL ANALYSIS

Estimation of statistical variables for analogue fault detectability evaluation p350

SWITCHING THEORY

Testability and test compaction for decision diagram circuits p153

THIN FILM GROWTH

Tunnelling current analysis of GaAs n^{++}-p^{++}-n^{++} ultrathin barrier structures grown by molecular layer epitaxy p218
Tunnelling currents in very thin planar-doped barrier n^{+}-i-p^{+}-i-n^{+} structures p31

TRANSFORMERS

Analysis of a hysteretic circuit containing an iron-cored inductor and a semiconductor switch p176